UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,788	06/06/2000	Heng-Ming Hsu	67,200-262	9280

7590 07/06/2007

Tung & Associates
838 W. Long Lake Road
Suite 120
Bloomfield Hills, MI 48302

EXAMINER	
TUGBANG, ANTHONY D	
ART UNIT	**PAPER NUMBER**
3729	

MAIL DATE	DELIVERY MODE
07/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/588,788	HSU ET AL.	
	Examiner	Art Unit	
	A. Dexter Tugbang	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,16-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,16-22,24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 3, 2007 has been entered.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 1, 4 through 6, 8 and 16 through 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haas 4,016,519 in view of Imai 5,834,825.

Haas discloses a method for fabricating an integrated circuit inductor comprising: providing a substrate (e.g. 3 in Fig. 1); forming over the substrate a planar spiral conductor layer (e.g. 1) comprising a single spiral to form a planar spiral inductor, wherein a successive series of loops within the planar spiral conductor layer is formed with a progressive and discontinuous variation progressing from a center of the spiral defined by a first loop to a periphery of the series of loops.

The successive series of loops forms a uniform ellipse and the series of loops forms progressive stepwise changes in line widths to form a series of discrete line widths for the successive series of loops (see Fig. 1).

Regarding Claim(s) 6, 16 and 18, Haas further teaches that the first loop defines the center of the spiral with a comparatively narrow line width and the final loop defines a perimeter with a comparatively wide line width where the progressive and discontinuous variation comprises progressively increasingly stepwise changes (see col. 2, lines 38-40).

Furthermore, Haas also teaches that the center of the spiral is defined by a first loop (in Fig. 1) that surrounds a planar surface (top surface of substrate 3) of the dielectric layer to define an inner cavity. The inner cavity of Haas can be read as a cavity formed by the planar surface (top surface of 3) of the dielectric layer and the first loop, or alternatively, can be read as hole (e.g. 4), which is defined by the first loop that surrounds the planar surface of the dielectric layer.

Regarding Claim(s) 8, Haas shows that the successive series of loops comprises a single spiral of 7 loops.

Haas teaches substantially all of the limitations of the claimed manufacturing method except that the substrate comprises a dielectric layer over a semiconductor substrate (as required in each of Claims 1 and 4).

Imai shows that it is known to manufacture planar inductors by forming a substrate with a dielectric layer (e.g. 11 in Fig. 5A) over a semiconductor substrate (e.g. 10) for several associated advantages. These advantages include:

1) to provide support for the planar spiral conductor layer (e.g. 12a) in the final structure;

2) to provide a degree of electrical isolation between the inductor and the planar spiral conductor layer (col. 2, lines 61-64); and

3) to allow accurate fine patterning of the planar spiral conductor layer (col. 2, lines 65-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the substrate of Haas by forming it with a dielectric layer over a semiconductor substrate, as taught by Imai, for anyone of, or all of, the associated advantages explicitly stated by Imai.

Regarding Claim(s) 5, Haas does not appear to mention that the planar spiral conductor layer is formed of a conductor material that is a non-magnetic metal. However, the examiner takes Official Notice that forming a planar spiral conductor layer with a non-magnetic metal is conventional, old, and notoriously well known in the art of forming inductors. As evidence of obviousness, the examiner cites Wollnik (U.S. Patent 4,187,485, col. 3, lines 30+) to show that a conductor material of a non-magnetic material (e.g. copper) can be used as the material for a spiral conductor layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Haas by utilizing a conventional non-magnetic metal of copper, as taught by Wollnik, for the advantages of inducing a magnetic field during operation of the inductor.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haas in view of Imai, as applied to claims 1 and 6 above above, and further in view of Murphy 5,844,451 and Esper et al 4,613,843.

Haas, as modified by Imai, discloses the claimed manufacturing method as relied upon above for Claims 1 and 6. The modified Haas method does not mention that the comparatively narrow line width is from 7 to 10 microns and that the comparatively wide line width is from about 17 to 21 microns.

Murphy teaches that line widths can be formed to dimensions up to 25 microns (col. 3, lines 62-64).

Esper teaches that line widths can be formed to dimensions of at least 4 microns.

Murphy and Esper show that comparative line widths of a planar spiral conductor can be formed between 4 to 25 microns as the values in between this range would be inclusive of the claimed ranges of 7 to 10 microns and 17 to 21 microns.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method Haas by forming the planar spiral conductor layer to a comparatively narrow line width from 7 to 10 microns and a comparatively wide line width from about 17 to 21 microns, as taught by Murphy and Esper, to perform the very same purpose of providing a planar spiral conductor layer to induce a magnetic field.

Alternatively, since Murphy and Esper teach upper and lower values for line widths of the planar spiral conductor layer, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the spiral conductor layer of Haas with a comparatively narrow line width from 7 to 10 microns and a comparatively wide line width from about 17 to 21 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haas in view of Imai, as applied to claim 1 above, and further in view of Romankiw et al 4,295,173 and Esper.

Haas, as modified by Imai, discloses the claimed manufacturing method as relied upon above for Claim 1 further including that the series of loops of Haas can be formed any other

types of shapes (col. 2, lines 22-25). The modified Haas method does not mention that one of those shapes can be a rectangle.

To form the planar spiral conductor layer is a series of loops with the shape of a rectangle is notoriously well known for the very same purpose of providing inductance with a Q value, or effecting the magnetic field, during operation. As evidence, the examiner cites Romankiw and Esper, each having rectangular shaped series of loops for the planar spiral conductor layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Haas by forming the series of loops with a rectangular shaped series, as taught by Romankiw and Esper, to perform the very same function of effecting the magnetic field and Q value of inductance during operation.

6. Claims 19 through 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the following four references..

a) Haas 4,016,519,

b) Church et al 4,219,584,

c) Imai 5,834,825, and

d) Wollnik 4,187,485.

Regarding Claim(s) 19 through 22, Haas teaches substantially all of the limitations of the claimed manufacturing method (as noted above) except for: 1) the substrate comprising a dielectric layer over a semiconductor substrate; and 2) that the variation comprises a series of progressive stepwise changes in spacings separating the successive series of loops.

Church discloses a method of making a planar inductor comprising: providing a substrate (e.g. 10 in Fig. 1); forming over the substrate a planar spiral conductor layer (e.g. 20)

comprising a single spiral to form a planar spiral inductor, wherein a successive series of loops within the planar spiral conductor layer is formed with a progressive and discontinuous variation progressing from a center of the spiral defined by a first loop to a periphery of the series of loops.

Church further teaches that the successive series of loops forms a uniform elliptical shape and the series of loops forms progressive stepwise changes in line widths to form a series of discrete line widths for the successive series of loops (see Fig. 2). The first loop of Church defines the center of the spiral with a comparatively narrow line width and the final loop defines a perimeter with a comparatively wide line width where the progressive and discontinuous variation comprises progressively increasingly stepwise changes along a vertical cross-section (see col. 2, lines 17+).

As with Haas, Church also does not teach: 1) that the substrate comprising a dielectric layer over a semiconductor substrate; and 2) that the variation comprises a series of progressive stepwise changes in spacings separating the successive series of loops.

Imai shows that it is known to manufacture planar inductors by forming a substrate with a dielectric layer (e.g. 11 in Fig. 5A) over a semiconductor substrate (e.g. 10) for several associated advantages. These advantages include:

1) to provide support for the planar spiral conductor layer (e.g. 12a) in the final structure;

2) to provide a degree of electrical isolation between the inductor and the planar spiral conductor layer (col. 2, lines 61-64); and

3) to allow accurate fine patterning of the planar spiral conductor layer (col. 2, lines 65-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the substrate of either Haas or Church by forming each of their substrates with a dielectric layer over a semiconductor substrate, as taught by Imai, for anyone of, or all of, the associated advantages explicitly stated by Imai.

Wollnik teaches that a series of loops separated by spacings can have a stepwise change in the variation of the spacings (see Figs. 6 and 7). Note the cross-sectional view (in Fig. 7) of Wollnik where the spacing between each of the loops changes in a decreasing variations (from left to right) or in an increasing stepwise variation (from right to left). The changes in spacing are based upon magnetic field intensity and current density (col. 2, lines 37+ and Figs. 2a, 2b) desired for the inductor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of either Haas or Church, by changing the variation of spacings between the loops in a series of loops in a stepwise change, as suggested by Wollnik, for the purpose of having a desired magnetic field intensity and current density of the inductor device.

Response to Arguments

7. Applicant's arguments filed on April 3, 2007 have been fully considered but they are not persuasive. The applicant(s) present numerous arguments with respect to the following topics and the examiner most respectfully disagrees for the following reasons.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *the principles*

of operation) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation came directly from the prior references themselves, each having a particular advantage and reason for success.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Dexter Tugbang whose telephone number is 571-272-4570. The examiner can normally be reached on Monday - Friday 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Dexter Tugbang/
Primary Examiner
Art Unit 3729

June 25, 2007